FIG.1

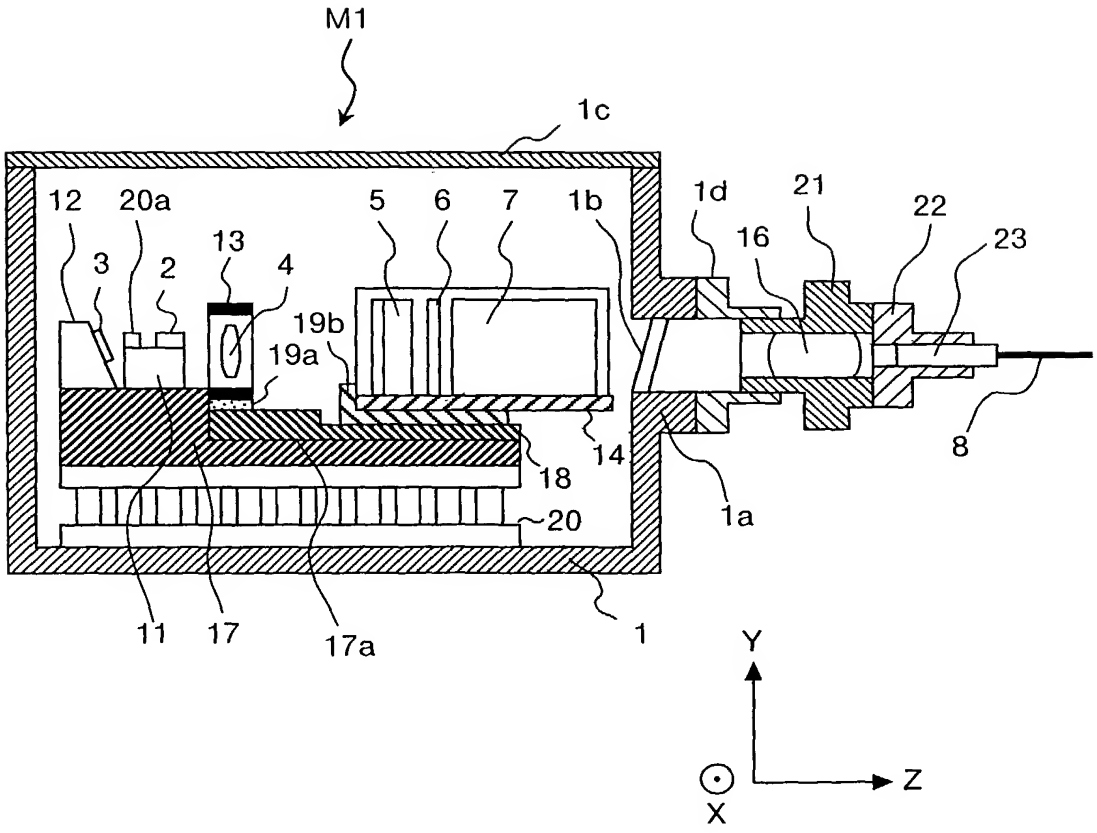
M1
1c
12
20a
13
3
2
4
5
6
7
1b
1d
21
16
22
23
19b
19a
14
8
18
1a
20
11
17
17a
1
Y
Z
X

FIG.2

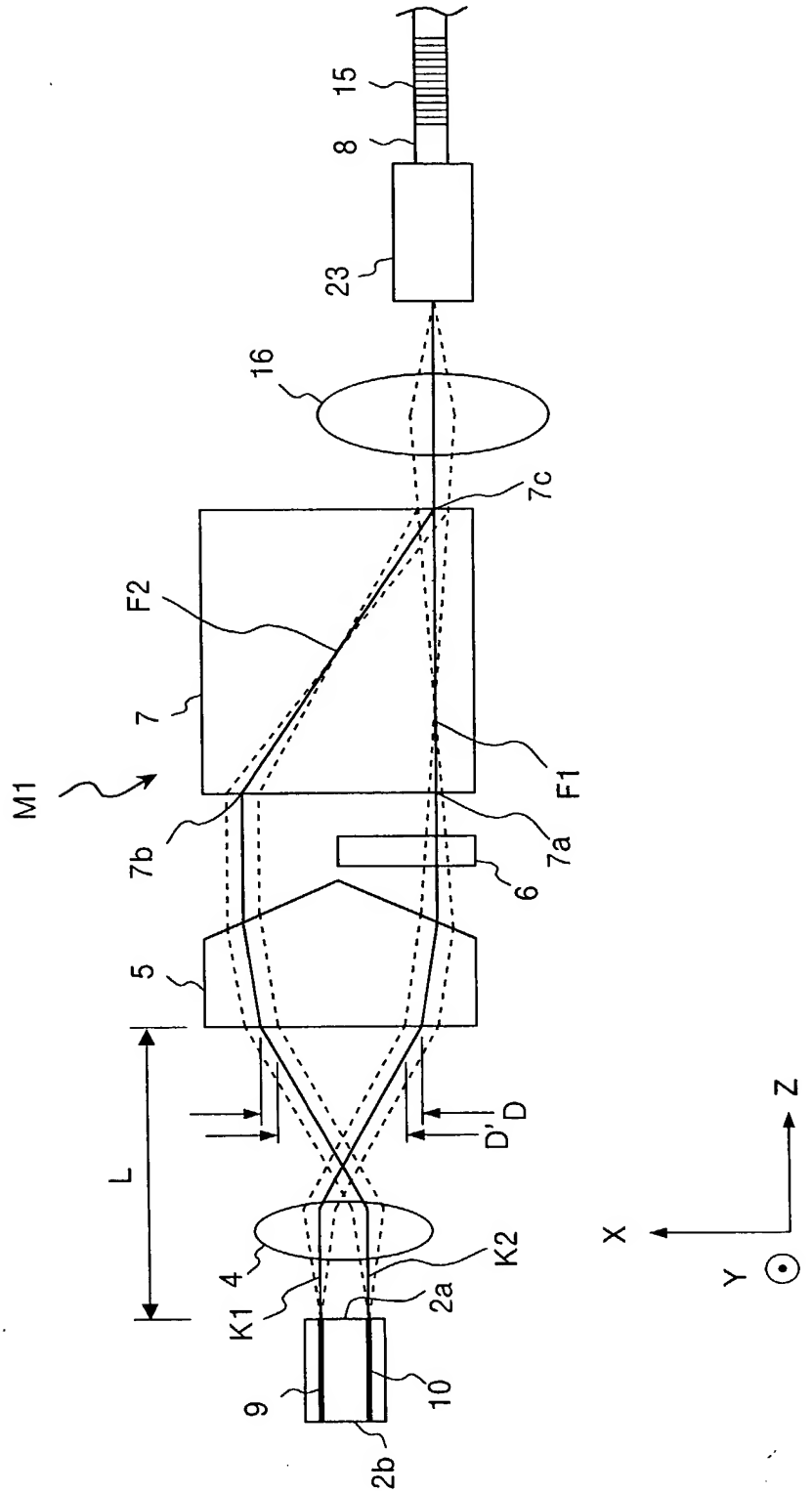

FIG.3A

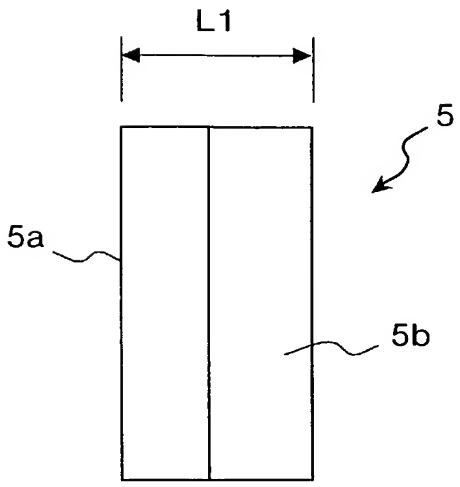

FIG.3B

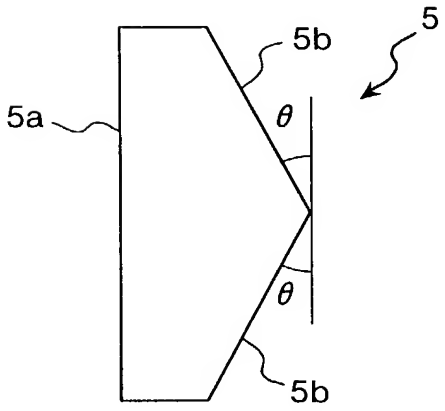

FIG.4A

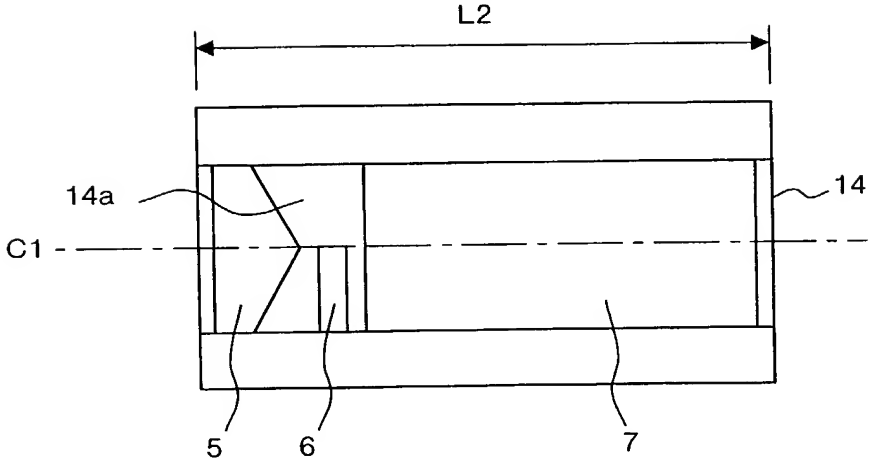

FIG.4B

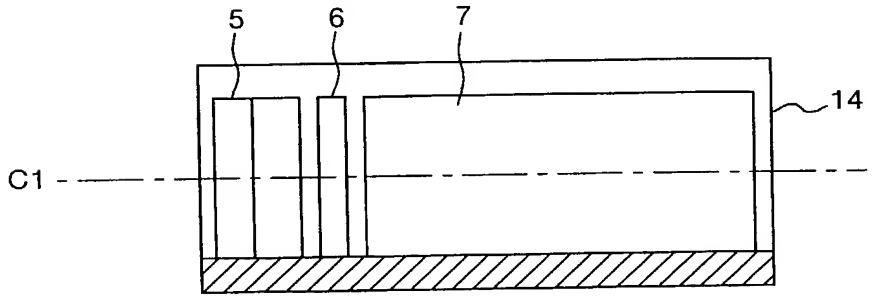

FIG.4C

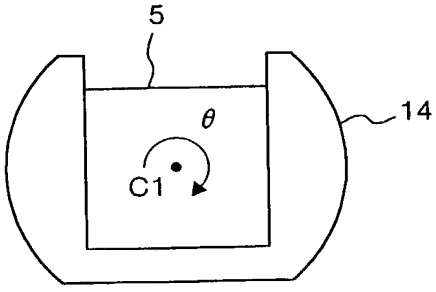

FIG.5A

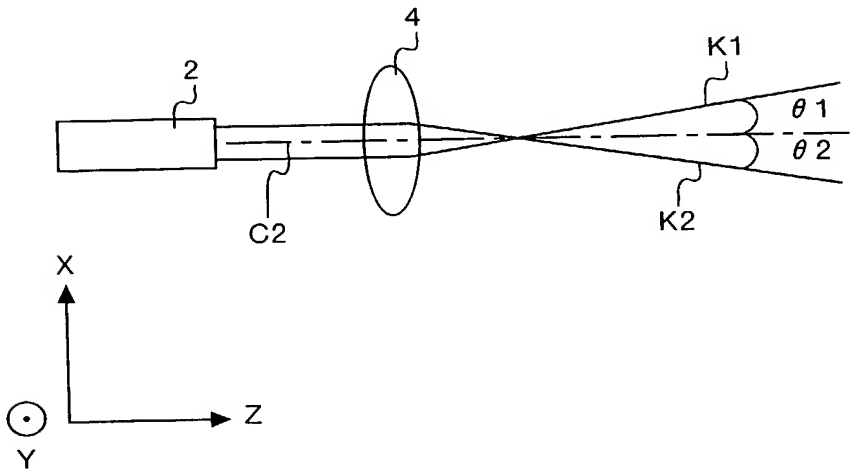

FIG.5B

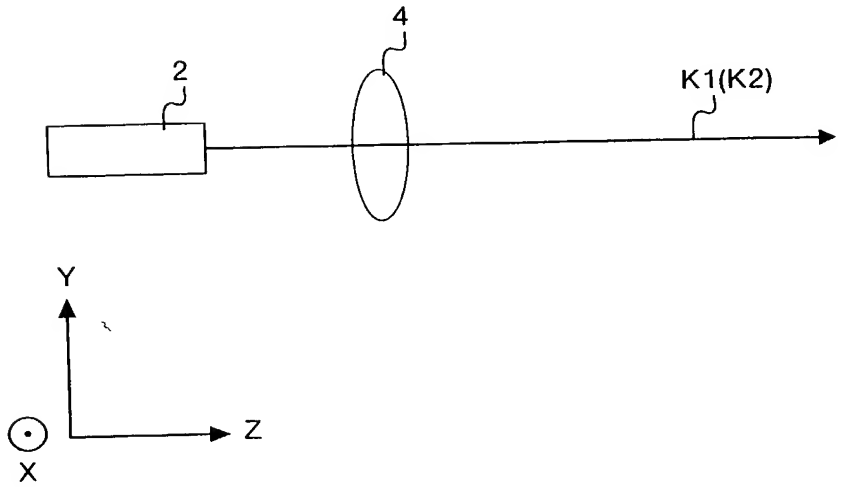

FIG.6A

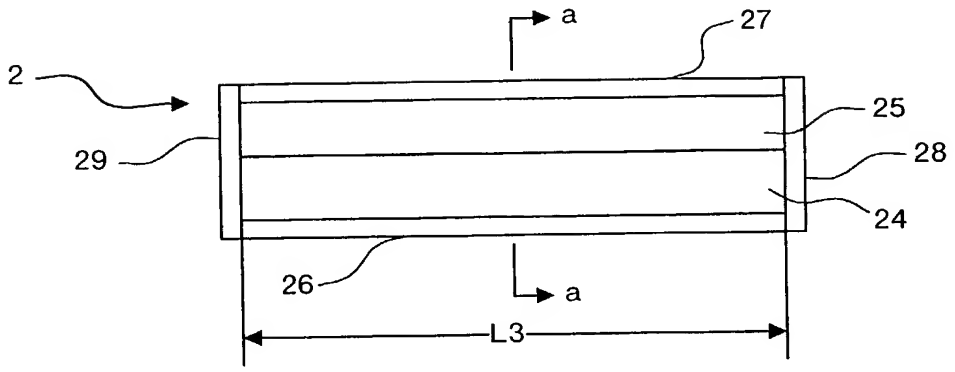

FIG.6B

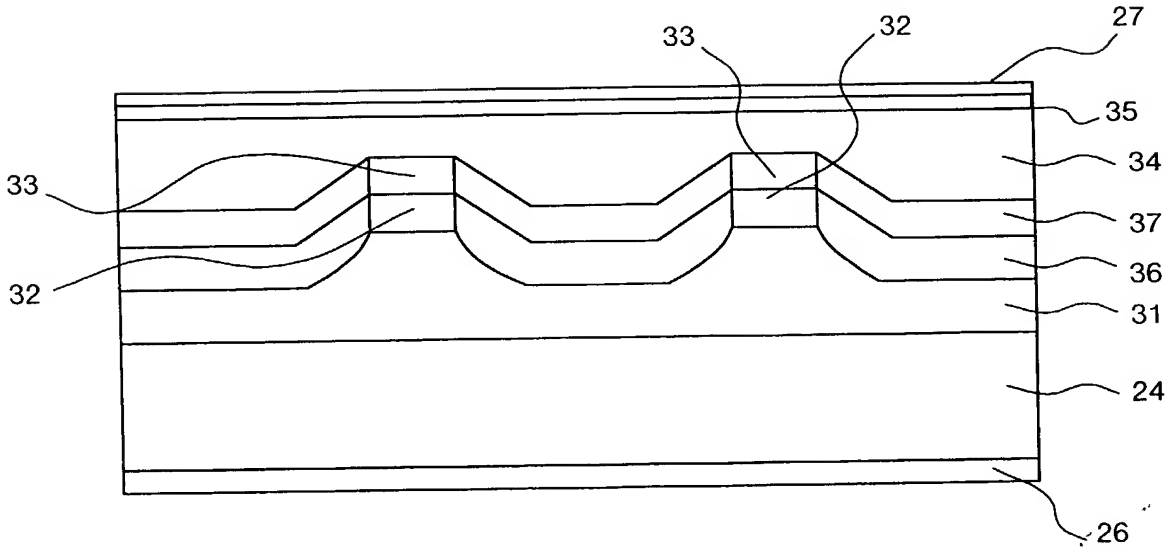

FIG.7

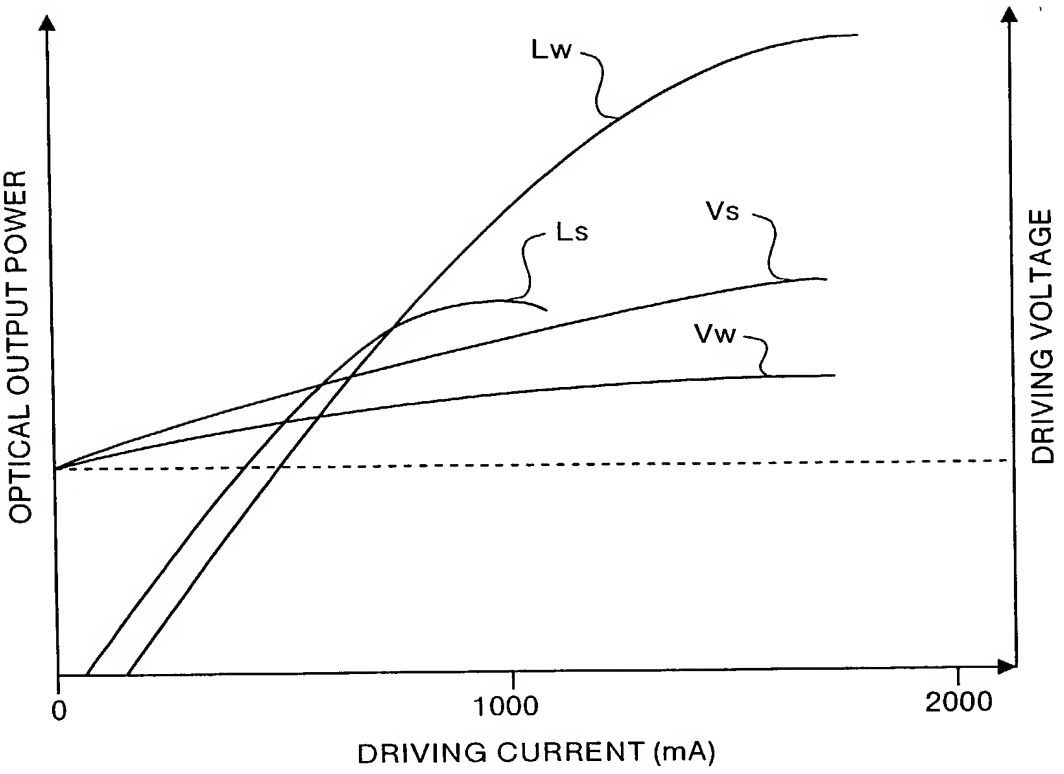
Lw
Ls
Vs
Vw
OPTICAL OUTPUT POWER
DRIVING VOLTAGE
0
1000
2000
DRIVING CURRENT (mA)

FIG.8

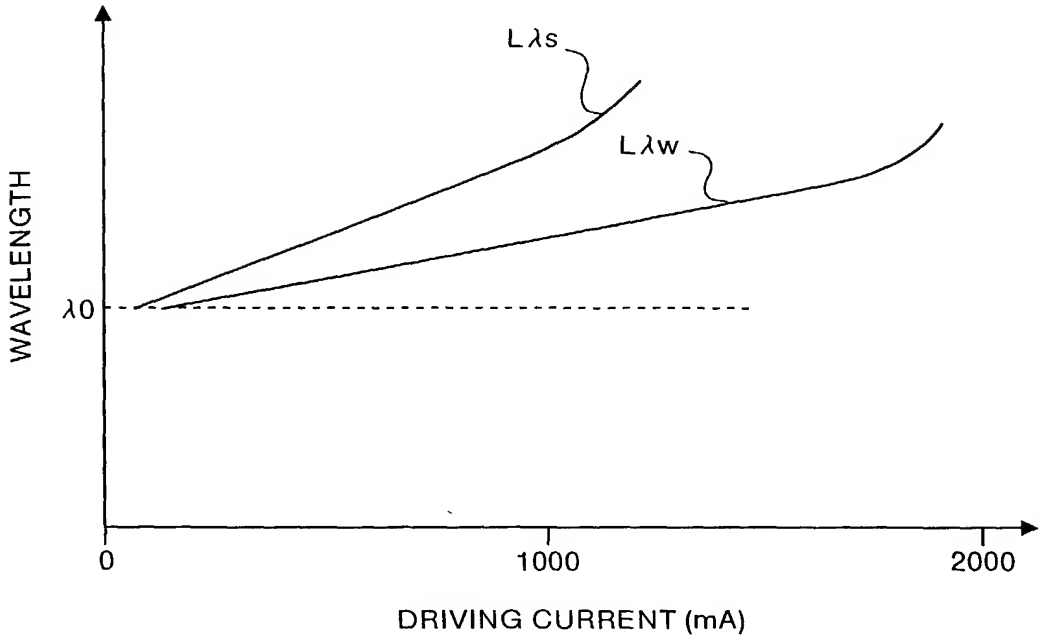

FIG.9

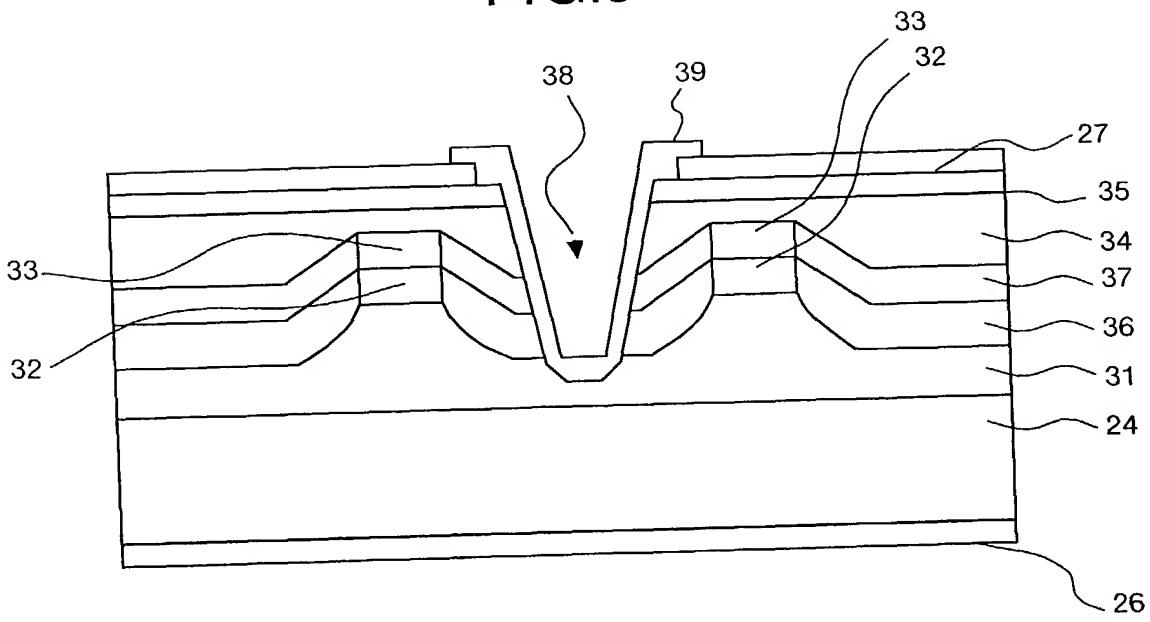

FIG.10

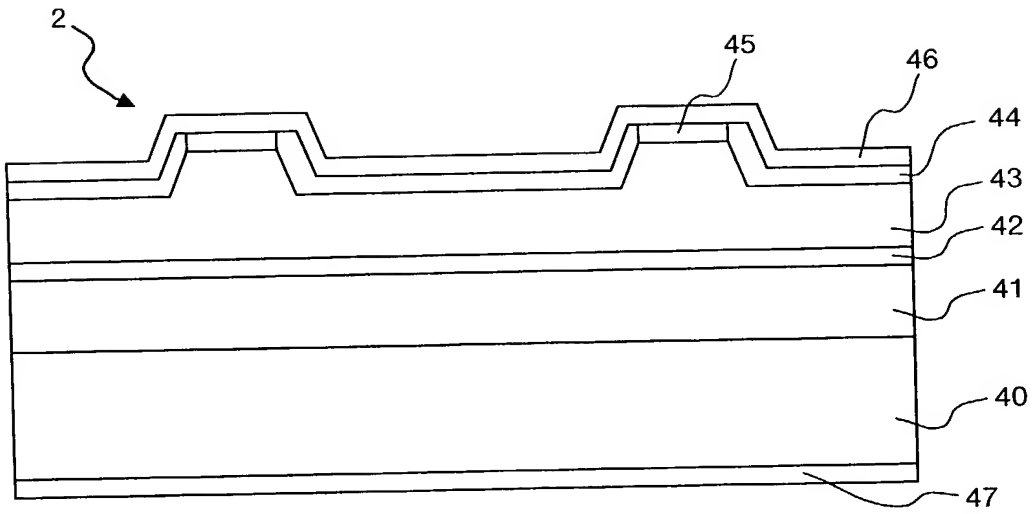

FIG.11

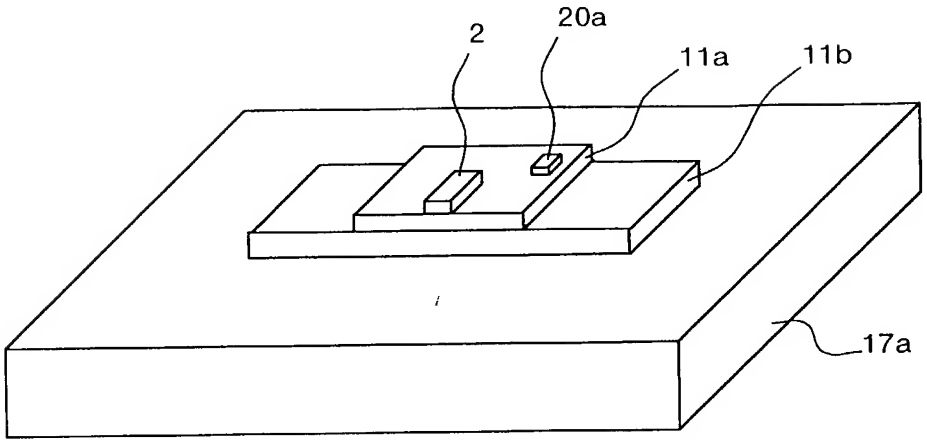

FIG.12

		A	B
UPPER HEAT SINK		CVD DIAMOND	AIN
LOWER HEAT SINK		AIN	AIN
HEAT OUTPUT [W]	LEFT ACTIVE LAYER	2.5	2.5
	RIGHT ACTIVE LAYER	2.5	2.5
TEMPERATURE [°C]	LEFT ACTIVE LAYER	37.96	49.53
	RIGHT ACTIVE LAYER	37.96	49.53
	UPPER MOUNT	26.76	26.77

FIG.13

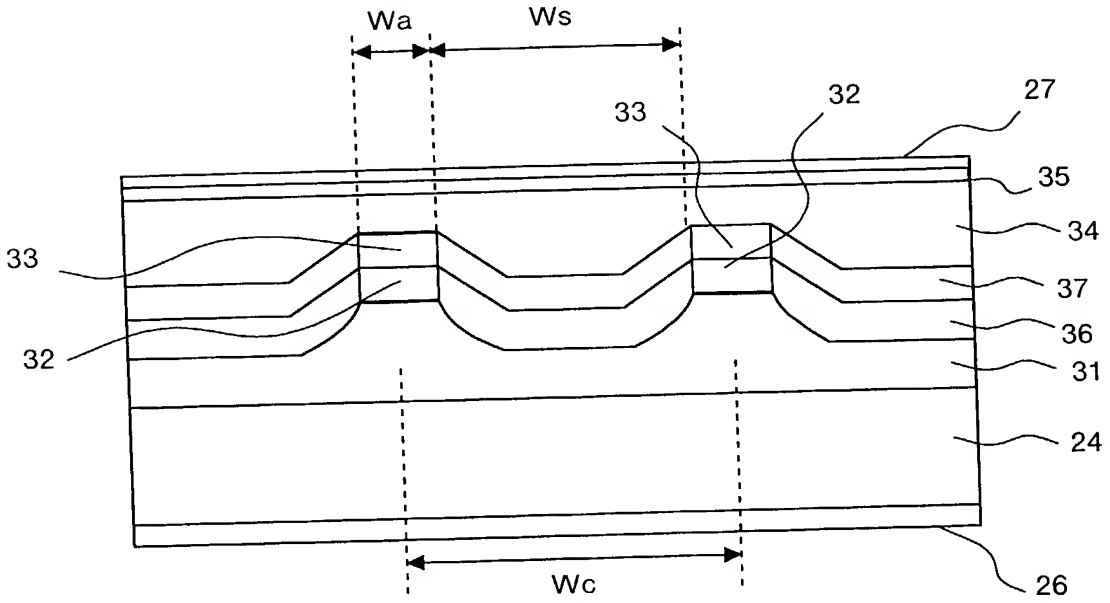
Wa
Ws
33
32
27
35
34
33
37
36
32
31
24
Wc
26

FIG.14

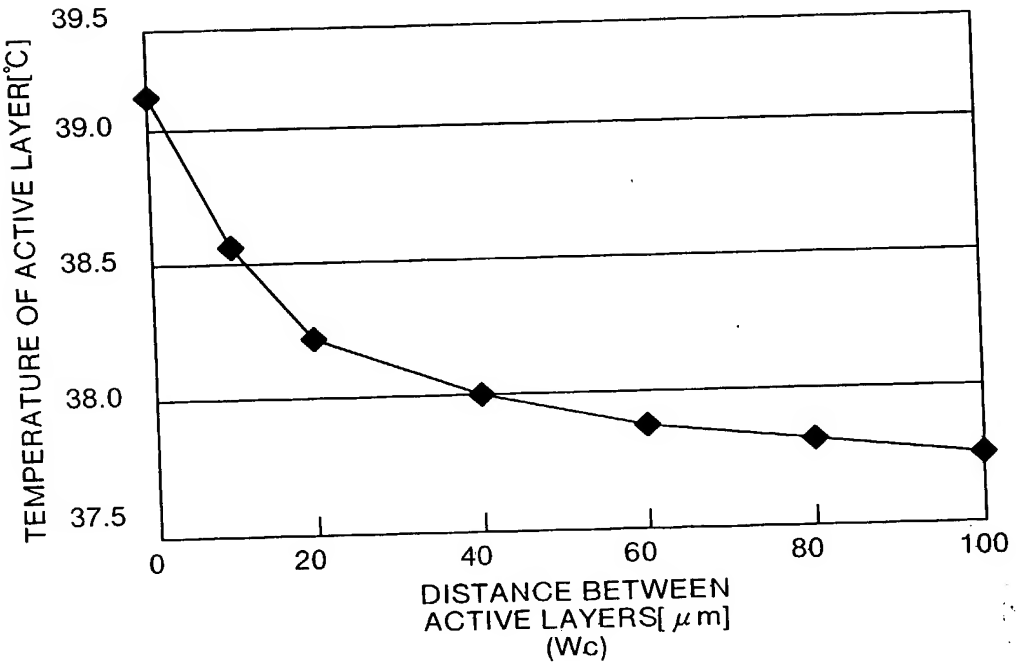
39.5
39.0
38.5
38.0
37.5
TEMPERATURE OF ACTIVE LAYER[°C]
0
20
40
60
80
100
DISTANCE BETWEEN ACTIVE LAYERS[μm] (Wc)

FIG.15

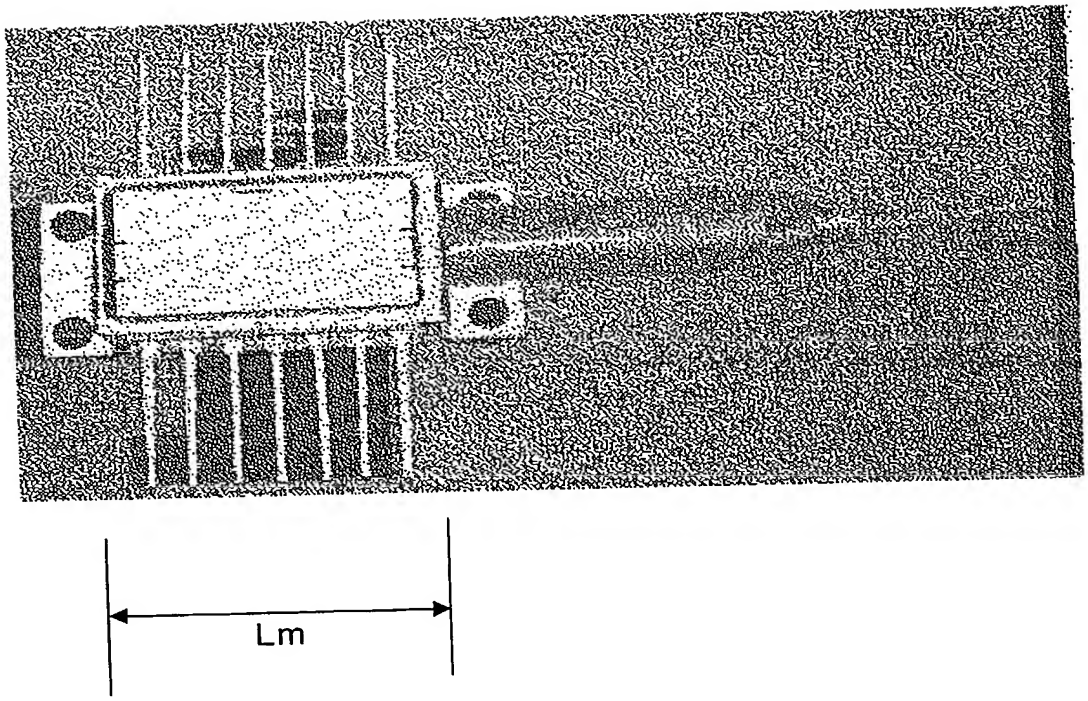

FIG.16

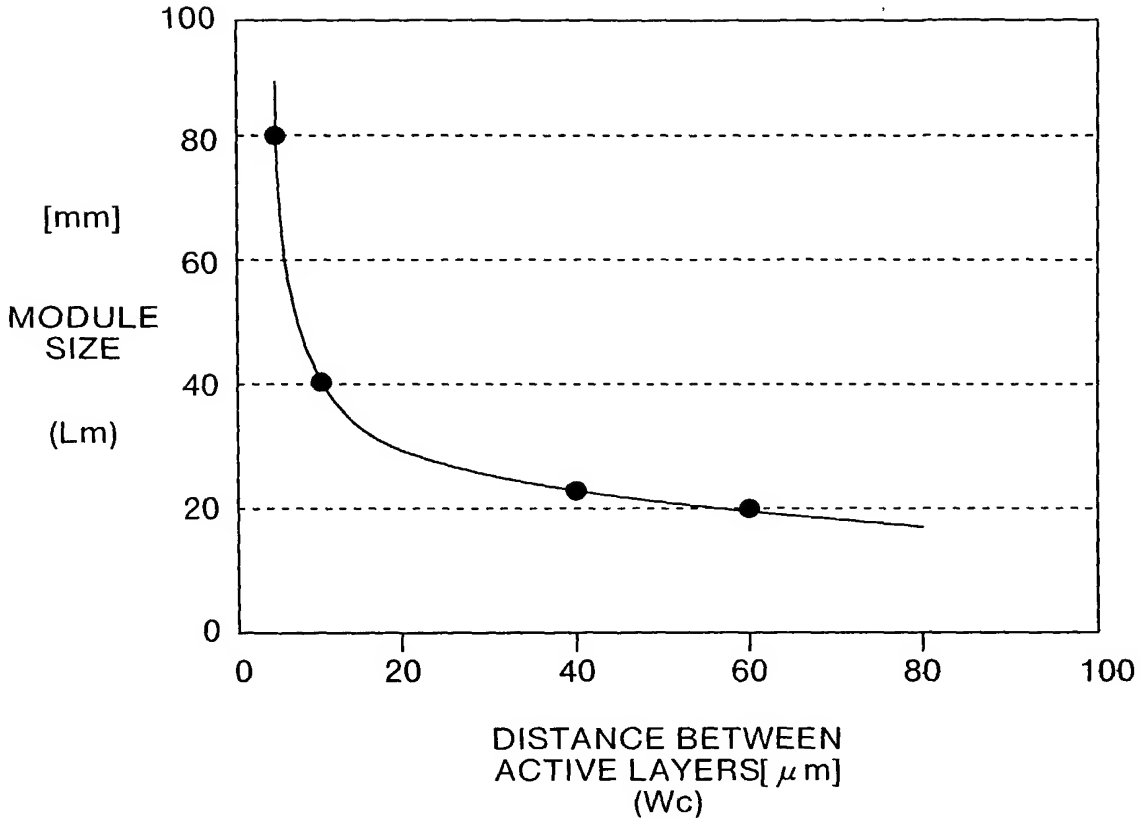
100
80
60
40
20
0
[mm]
MODULE SIZE
(Lm)
0
20
40
60
80
100
DISTANCE BETWEEN ACTIVE LAYERS[μm]
(Wc)

FIG.17

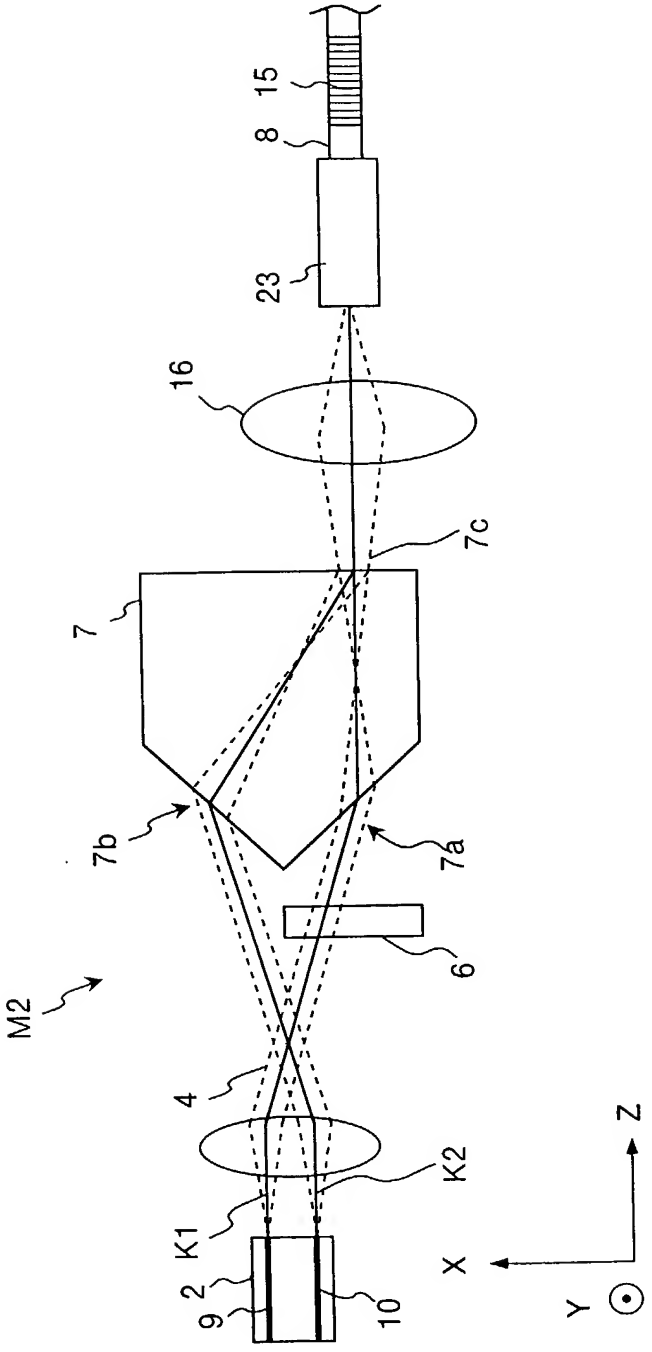

FIG.18

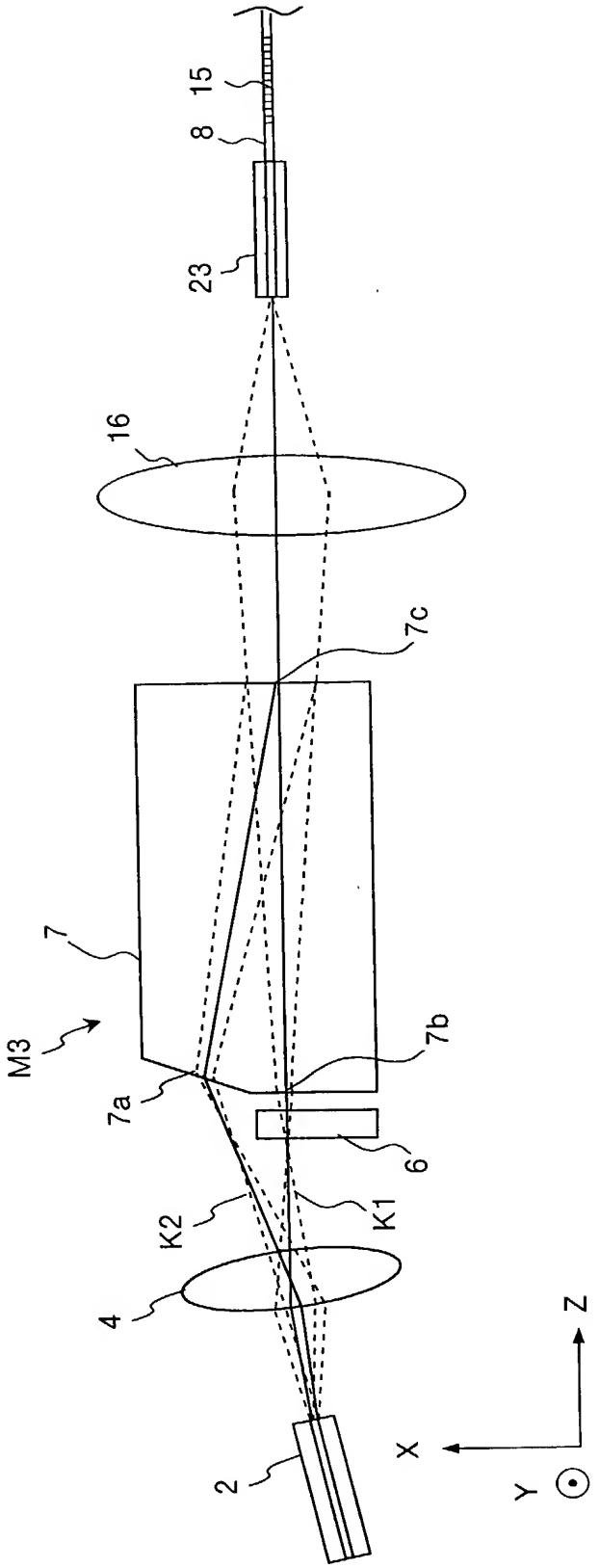

FIG.19

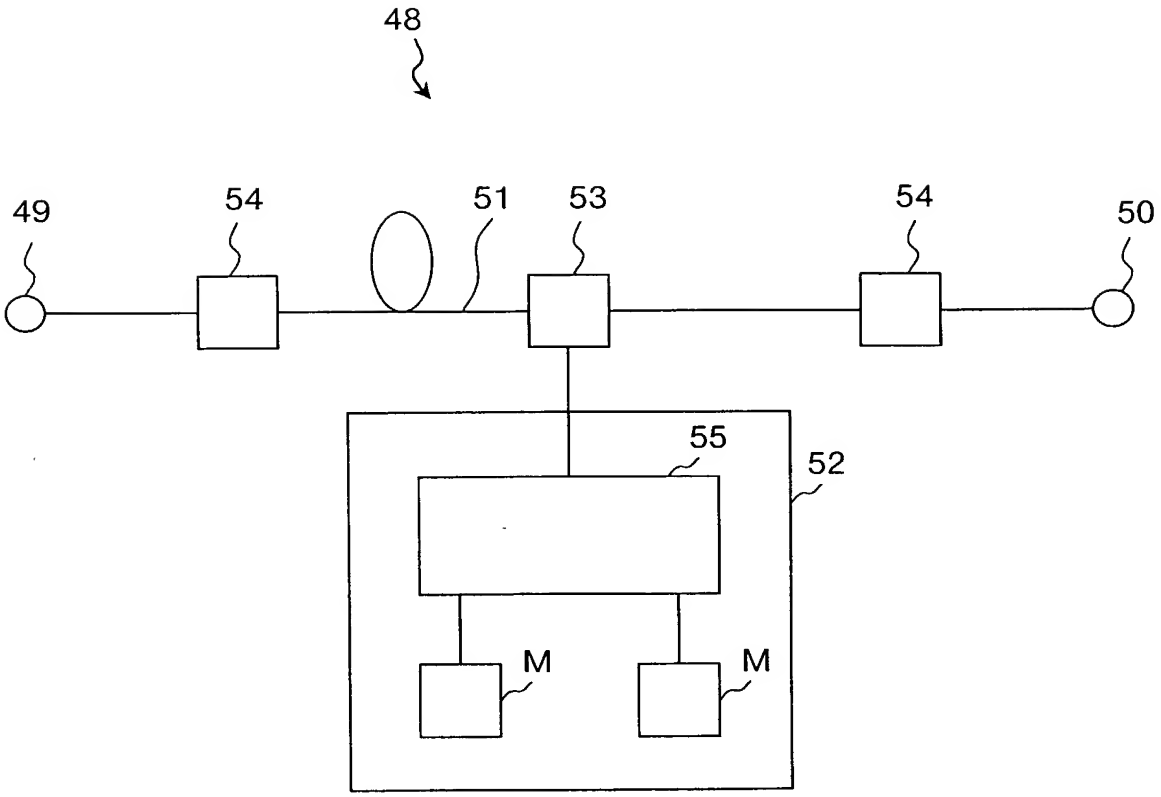

FIG.20

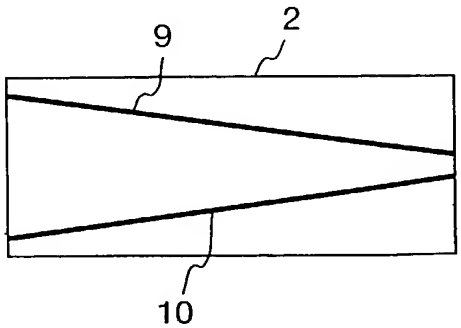

FIG.21